[0019] One skilled in the art will recognize that FIG. **1** illustrates an ideal profile as doped. The distance SEC may vary after subsequent diffusion processes. The distance SEC shown in FIG. **1** is used to illustrate the inventive aspects of the various embodiments. The present invention is not limited to any particular distance between two high voltage P type implanted regions.

[0020] In an embodiment, SEC is an adjustable parameter. As shown in FIG. **1**, SEC represents the distance between two high voltage P type implanted regions, namely **108** and **110**. More particularly, SEC is the distance from an edge **122** of the first high voltage P type implanted region **108** to an edge **124** of the second high voltage P type implanted region **110**. In a semiconductor doping process, the doping material may be added via ion implantation. By controlling the doping range of a high voltage P type implanted region (e.g., **108**), SEC may change accordingly. As discussed below with respect to FIG. **3**, SEC helps to provide an adjustable threshold voltage of ESD protection.

[0021] It should be noted that the doping technique used in the previous example is selected purely for demonstration purposes and is not intended to limit the various embodiments of the present invention to any particular doping technique. One skilled in the art will recognize that alternate embodiment could be employed (such as employing the diffusion technique).

[0022] In FIG. **1**, the ESD protection structure **100** provides an on-chip ESD protection solution. For ESD protection applications, the second P+ region **104** is typically coupled to an input/output (I/O) pad and the first P+ region **102** is typically coupled to a power supple VSS pad, which is typically grounded or coupled to a power supply. An advantageous feature of the described embodiment is that the adjustable threshold voltage of an ESD protection device allows different voltage ESD protection schemes derived from the same structure as illustrated in FIG. **1**.

[0023] FIG. **2** illustrates an equivalent circuit diagram of the ESD protection structure **100** illustrated in FIG. **1**. An equivalent circuit **200** of the ESD protection structure **100** illustrated in FIG. **1** includes a bipolar PNP transistor **202** having an emitter **204**, a base **210** and a collector **206**. The base **210** is coupled to the N+ region **116** through a resistor **206**. The resistor **206** represents the parasitic resistance in the HVNW **106** (not shown but illustrated in FIG. **1**). The emitter **204** is formed by the second P+ region **104** and the second high voltage P type implanted region **110**. The collector **206** is formed by the first P+ region **102** and the first high voltage P type implanted region **108**. Referring again to FIG. **1**, the second high voltage P type implanted region **110** and the second P+ region **104** have the same conductivity type but different doping concentrations. The second high voltage P type implanted region **110** extends the second P+ region **104** to a deeper region. Likewise, the first high voltage P type implanted region **108** extends the first P+ region to a deeper region. The extensions of the emitter **204** and the collector **206** of the bipolar PNP transistor **202** result in a change of the breakdown voltage characteristic between the emitter **204** and the collector **206**.

[0024] In sum, a simplified circuit diagram **200** depicts that the corresponding circuit of the ESD protection structure **100** constitutes one bipolar PNP transistor (e.g., **202**), wherein both its emitter and collector are formed by a P+ region (e.g. **104**) and a high voltage P type implanted region (e.g., **108**) disposed underneath the P+ region. However, it should be recognized that while FIG. **2** illustrates the ESD protection circuit with one bipolar PNP transistor (e.g., PNP transistor **202**), the ESD protection circuit could accommodate any numbers of bipolar PNP transistors. Furthermore, it is understood that the ESD protection circuit may be implemented using a plurality of bipolar PNP transistors in series connection. On the other hand, other configurations of a plurality of bipolar PNP transistors such as parallel-connected bipolar PNP transistors coupled to parallel-connected bipolar PNP transistors are also within the contemplated scope of this embodiment.

[0025] The ESD protection circuit **200** is typically placed at an I/O pad and a VSS of a device to be protected (not shown but illustrated in FIG. **8**). The second P+ region **104** is typically coupled to the I/O pad and the first P+ region **102** is typically coupled to the VSS, which is typically grounded or coupled to a power supply. If an ESD event occurs, a voltage spike is applied between the second P+ region **104** and the first P+ region **102**. Consequently, the bipolar PNP transistor **202** experiences the voltage spike, which may exceed the bipolar PNP transistor **202**'s breakdown voltage. As a result, the bipolar PNP transistor **202** enters an avalanche conduction mode. As a consequence of the avalanche conduction, the bipolar PNP transistor provides a current path so that the ESD discharge current can flow from the emitter **204** to the collector **206**. The conduction of the bipolar PNP **202** clamps the voltage between the emitter **204** and the collector **206** to a lower level so that the internal circuits coupled to the emitter **204** can be protected.

[0026] Referring again to FIG. **2**, the base **210** is coupled to the emitter **204** through a resistor **208**. In this embodiment, the resistor **208** represents the body resistance of the HVNW **106**. It should be noted that the resistance between the base **210** and the emitter **204** may have an impact on the collector-emitter breakdown voltage of the bipolar PNP transistor **202**. The direct connection between the N+ region **116** and the second P+ region **104** is provided for illustrative purpose only, and is provided only to provide an example of the functionality that may be included in this embodiment. One of ordinary of skill in the art will realize that in ESD protection applications, the N+ region **116** may be floating or coupled to the second P+ region **104** through an external resistor outside the ESD protection structure **100**.

[0027] FIG. **3** shows three curves illustrating the current versus voltage characteristics of the ESD protection circuit **200** with different SEC values. The horizontal axis of FIG. **3** represents the ESD voltage across an ESD protection circuit (e.g., the ESD protection circuit **200**). The vertical axis of FIG. **3** represents the ESD current flowing through the ESD protection circuit. A curve **302**, a curve **304** and a curve **306** illustrate the currents flowing through the ESD protection circuit **200** having a SEC of 1.6 um, 2 um and 2.5 um respectively.

[0028] As shown in FIG. **3**, the breakdown voltages for curves **302**, **304** and **306** are quite similar (approximately 15V). Once the applied ESD voltage exceeds the breakdown voltage, three ESD currents increase in proportion to the applied ESD voltage. However, at the same ESD current level, a different SEC value causes the ESD protection circuit **200** to have a different holding voltage. For example, when the ESD protection circuit **200** having a SEC of 1.6 um (illustrated by curve **302**) provides an ESD current of 0.004, the corresponding holding voltage is slightly over 20V. By contrast, with the same ESD current level, the ESD protection circuit **200** having a SEC of 2.5 um (illustrated by curve **306**) has a holding voltage of about 23V. Similarly, when the ESD protection circuit **200** has a SEC of 2 um, the curve **304** illustrates the hold voltage is about 21.5V.

[0029] FIG. **3** shows an ESD protection device based upon the ESD protection structure **100** can have different holding